10/707,774 Remarks.

1. Following are some amendments to the specification. It is mostly the correction of typographical errors. No new matter has been added. Bold text in brackets [–] was added to point out certain of the additions that may be hard to see, for example, a period ".".

Some matter was also more clearly defined for the benefit of the claims. Each instance is discussed below in the context of the response to specific points in the office action.

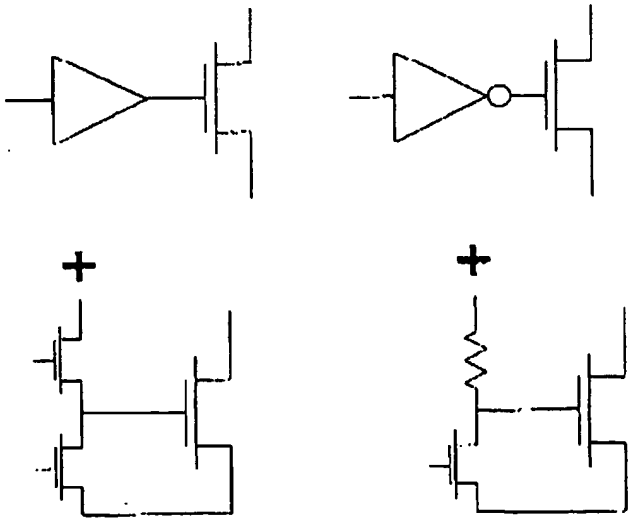
2. Application 10/248,438 is abandoned.

3. I have amended the claim 1 to overcome your objection. It was a typographical error requiring a deletion, so no new matter has been added.

I have also amended claim 12 to correct a typographical error. No new matter has been added.

I have also amended claim 13 to be a method claim. This is discussed further below.

4. The schematic elements shown below for turning MOSFETs off and/or on are very commonly used in circuit design, and there is no intent to claim these and variants of them as being novel. In addition, it is well known to use a MOSFET connected to a negative voltage to turn off a MOSFET more rapidly.



Claim 1 and 12 relate entirely to an apparatus and method for the very fast turn off of MOSFETs.

Claim 1 has the following recitation of structure:

"a first MOSFET having a gate, a drain and a source for switching a load current equal to I_d;

at least a second MOSFET having a gate, a drain and a source for turning off the first MOSFET;

the source of the first MOSFET and the source of the at least a second MOSFET being connected together as a source connection;

the gate of the first MOSFET and the drain of the at least a second MOSFET being connected together as a drain-gate connection; "

None of the above are points of novelty in the claims.

Claim 1 introduces the points of novelty in the following:

"the gate of the first MOSFET being characterized by having a very low gate resistance;

the on resistance of the at least a second MOSFET being characterized by having a very low channel resistance;

the source connection being characterized by having a very low impedance: and

the drain-gate connection being characterized by having a very low impedance"

These points introduce the novel points of the invention, but by themselves are indefinite, as "very low gate resistance", "very low channel resistance", and "very low impedance" (two instances), by them selves are indefinite.

Claim 1 then states that a current will flow:

> "so that
> when the at least a second MOSFET is turned on, a gate current i_g will flow from the gate of the first MOSFET to the source of the first MOSFET through the at least a second MOSFET,"

No point of novelty is presented in this clause, as it is the necessary result of turning on the at least a second MOSFET.

In claim 1, the indefinite "very low gate resistance", "very low channel resistance", and "very low impedance" (two instances), are made definite and the principle point of novelty is taught in the final clause of claim 1.

> "and the gate current i_g is larger than the load current i_d."

The significance of this is found in paragraph [0046], but note that [0046] is amended in this response to be two paragraphs, the second beginning with "Figure 3 —". Note also that typographical errors are also corrected in [0046].

Please also see [0056] through [0058] for a further explanation of the importance of having a gate current I_g that is higher than the drain current I_d, and the

importance of having a "very low gate resistance", "very low channel resistance", and "very low impedance" (two instances) in the gate drive circuit.

The specific relationship required is defined in [0084]. It is also recited in claim 12 more specifically, as follows.

> "such that the very low gate resistance [[if]] of the first MOSFET plus the very low on resistance of the at least a second MOSFET plus the very low resistance of the source to source connection plus the very low resistance of the gate to drain connection is less than the ratio of V_{th} to I_d."

Claim 1 might be improved by the inclusion of a similar clause, but in view of Festo, I am reluctant to propose such an amendment. Because this is a necessary condition for the gate current I_g to be greater than the drain current I_d, the recitation of a gate current I_g which is higher than the drain current I_d in the last line of claim 1 includes this requirement.

I have amended [0084] to define this more clearly. This amendment merely states the previously recited conditions for the sum of the impedances and/or resistances in the gate drive circuit as a definition for the specification and the claims, and is not new matter.

This condition of making a gate drive circuit with sufficiently low impedance is not easily achieved, and I believe that it is a fair and accurate statement that it could not be achieved by any prior art known to one having ordinary skills in the art of

power converters at the time that this invention was made. Some reasons to support his assertion follow:

1. No separately packaged gate drive and MOSFET can have a sufficiently low gate and source leakage inductance (impedance) to use this invention. Even the co-packaged but separate chip schemes, like figures 7 and 9, are marginal, probably suitable only for the least demanding applications or for breadboard testing. Accordingly, no prior art that uses separately packaged gate drive and MOSFETs would suggest this invention to one of ordinary skill in the art of power converters.

2. The "Miller effect" characteristics of MOSFETs is so widely accepted that one having ordinary skill in the art of power converters at the time that this invention was made would not believe that it was possible, let alone obvious, to be overcome by using a gate drive I_g that was larger than the drain current I_d. While I have not done an exhaustive search of the literature, I have attended a number of conferences where the problems of MOSFET gate drives was a frequent topic of the papers presented. I am generally familiar with manufacturer's application notes, and I read periodicals that cover power converter design and manufacturer. Never have I seen any suggestion that overcoming the Miller effect was possible or desirable.

3. It is widely believed by those having ordinary skills in the art of power converter design that the switching speed of a MOSFET must be limited by limiting the gate drive to control noise, or electro-magnetic interference (EMI). Thus it would not be obvious to those having ordinary skills in the art of power converters that there would be an advantage of using switching speeds in the order of nanoseconds or fractions of a nanosecond, see [0041].

4. Commercially available MOSFETs at the time that this invention was made did not, as a generalization, have sufficiently low gate resistance to use this invention, even if all other of the circuit resistances and impedances were ideal. The gate mesh resistance itself is high enough so that the required high gate current I_g could not be achieved by short-circuiting the gate lead to the source lead. While some cells of the MOSFET might be sufficiently close to the gate and source leads, as a generalization, the gate mesh resistance together with the gate capacitance of the respective gate cells comprise a distributed RC-RC-RC network having significant propagation delay as well as attenuation, limiting the voltage fall time of the gates of the MOSFET cells furthest from the gate leads. This invention teaches MOSFETs that have features, believed to be novel, to lower the effective gate mesh resistance and propagation delay. None of the prior art know to me has or suggests these features.

5. Commercially available MOSFET gate drivers at the time that this invention was made, did not, as a generalization, have sufficient drive capacity or a sufficiently low impedance to sink gate currents I_g from the gate of the MOSFET which were larger than the drain current I_d. While numerous custom gate drive circuits are used, I am not aware of any that suggest a current capability greater than the drain current with the speed required to use this invention. Not only must the MOSFET gate driver have the necessary low on resistance, it must also have a high pinch-off current, higher than the highest anticipated drain current.

6. A principle use for MOSFET switches is in power converters, and in an important class of power converters, the MOSFET switches interface with transformers, either as primary side switches or as synchronous rectifiers. Transformers have significant leakage inductance, which means that significant energy will be stored in the leakage inductance of the transformer windings and this energy will have to be dissipated when the circuit is interrupted by turning off the MOSFETs. In many circuits, the time that it takes to dissipate the stored energy in the leakage inductance will define a minimum off time, and therefore a maximum duty cycle that the circuit can achieve. This became a barrier to increasing the switching frequency of transformer coupled circuits, and without increased frequency, there was little perceived reason to switch faster. In fact, it was common practice to slow the switching speed to control noise (EMI).

The invention of the cellular transformer (10/708,846) and the coaxial push pull transformer (10/904,371) changed that, in that the leakage inductance is greatly reduced in these transformers. These transformers have not been disclosed publicly, so no one having an ordinary skill in the art of power converters has knowledge of them. Accordingly, there has been little incentive to study and invent MOSFET gate drive methods to switch in nanoseconds or fractions of a nanosecond. Commercially available transformers could not use this invention to advantage.

With specific reference to Parks (USP 6,208,535), figure 6a shows a MOSFET using an IRFP250 as an example being turned off by two MOSFETs using two TN07s as an example. While the interconnections resemble that of the present invention and the current flows are similar, the requisite very low impedances are not shown, nor is there any text in the specification contemplating that the gate current would exceed the drain current at the moment of turn off. The TN07, made by Supertex, Inc., has an on resistance of 1.3 ohms, so that the pair would have a resistance in parallel of 0.65 ohms. and a current rating of 1 amp (pulsed), so that the current rating of the parallel pair would be just 2 amps. The IRFP250, made by International Rectifier and others has a drain current rating of 33 amperes. It is thus apparent that there is no capability of the circuit to have a gate current that is larger than the drain current, and there is no suggestion in the specification that this was an objective, unrealized or not.

Therefore, with respect to claims 1 and 12, Parks does not disclose a schematic capable of having a gate current larger than the drain current, nor does Parks disclose that as an objective, unrealized or not.

In as much that claims 1 and 12 of this invention contemplate the turn off of a MOSFET, with no restrictions on the drain current, the gate drive circuit must be capable of providing a gate current that is larger than the drain current at its maximum design current. What the relative gate and drain current might be in another condition (as when the IRFP250 is off) is not relevant to claims 1 and 12. As an aside, however, since the gate has the characteristics of a capacitor, the gate current will be zero when the IRFP250 is off (steady state).

As to claim 2, not withstanding that the limitation of claim 1 that the gate current is larger than the drain current is not realized, two TN07 is not, in my opinion, a "large number" nor does it suggest a "large number".

As to claim 3, not withstanding that the limitation of claim 1 that the gate current is larger than the drain current is not realized, Parks does not show any of the circuit components integrated into a MOSFET die.

As to claim 8, the limitation of claim 1 that the gate current is larger than the drain current is not realized, and cannot be realized with the components shown. The resemblance to the turn on circuit that is added does not override that limitation.

As to Kinzer, no novelty is claimed for a driver die mounted upon a MOSFET die. There are many familiar examples of this technology in use, dating back many years.

In column 1, line 30 and following, Kinzer recites as an example the IRF7811W MOSFET, made by International Rectifier. This MOSFET is rated for 11.2 amps at 90 degrees C. In column 1, line 34, Kinzer gives as an example that the IRF7811W may require a gate current of 1.4 amps for a switching speed of 10 nanoseconds.\

The gate resistance specified for the IRF7811W is 1.8 ohms, and in every drawing of Kinzer, the gate of the first MOSFET is shown as a single small gate pad. The gate threshold voltage specification for the IRF7811W is 1.0 volts, so even with a perfect (zero impedance) gate drive, the highest gate current that can be achieved with the circuit structure of claims 1 and 12 of the present invention is 0.55 amperes. Given the current rating of the IRF7811W of 11.2 amperes, it is likely that it would be used with at least 5.5 amperes operating current and that is the drain current at the moment that the MOSFET is turned off. It is apparent that the components shown miss the criteria that the gate current be larger than the drain current by an order of magnitude.

In as much that claims 1 and 12 of this invention contemplate the turn off of a MOSFET, with no restrictions on the drain current, the gate drive circuit must be capable of providing a gate current that is larger than the

drain current at the maximum design current rating of the power converter in which it is used. What the relative gate and drain current might be in another condition (as when the transistor 1 is off) is not relevant to claims 1 and 12. As an aside, however, since the gate has the characteristics of a capacitor, the gate current will be zero when the transistor 1 is off (steady state).

As to claims 2 through 6 being unpatentable over Kinzer in view of Parks, no novelty is claimed in the present invention for either a plurality of second MOSFETs (Parks) nor the location of one or a plurality of second MOSFETs on the MOSFET die (Kinzer). Neither Parks nor Kinzer teach or anticipate the limitations of the parent claim 1, and these limitations carry through to the dependent claims 2 through 6.

As for claim 13 being unpatentable over Lee (USP 6,127,861) in view of Wanlass (USP 3,356,858), the present invention differs from Lee and is patentably distinct for the reasons recited in paragraph [0114] of the specification. No novelty is claimed for the schematic structure itself of having parallel MOSFETs, each with their own driver. Besides Lee, this is a widely used circuit for increasing the power capability of a power converter. Rather, the novelty in this invention lies in the relative size of the first and second MOSFETs and in their sequential operation so as to reduce or eliminate the effects of the Miller current.

A distinction in claim 13 is

"The first MOSFET being larger than the second MOSFET"

noting that the size of the MOSFET is as defined in paragraph [0110] of the specification.

However it seems that a distinction over prior art is in the sequencing of the turn off, and I have failed to recite a sequencing means. Further, no sequencing means is disclosed in the specification. Accordingly, I am amending claim 13 to be a method claim, including the method steps of turning the MOSFETS off in the correct sequence. This is not new matter, as the sequence for turning off the first and second MOSFETS (by turning on the third and fourth MOSFETS) is clearly explained in [0111] through [0113].

Note that no novelty is claimed in claim 13 for the recitation of the structure to which the method is applied, even though "the first MOSFET being larger than the second MOSFET" is a novel feature of the structure. No apparatus is recited for turning on the third and fourth MOSFETs, but one having ordinary skill in the art of power converters would know what it means to turn on a MOSFET, and one having ordinary skill in the art of power converters would know how to do so by applying a charge to the gate of the MOSFET, and they would also know how to construct gate driver and control circuits to do this. Thus one having ordinary skill in the art of power converters would be able to use the invention without undue experimentation.

In addition, the indefinite criteria "low voltage" is replaced with the definite criteria "voltage that is below the cutoff threshold gate voltage of the first MOSFET". This is not new matter, see paragraph [0112].

As to claims 9-11 being objected to as being dependent on claim 8 which is dependent on claim 1, I believe that the rejection to claim 1 (and thus claim 8) has been overcome and that these claims 9-11 are now allowable.

I believe that the above explanations and amendments overcome the rejections and objections of the claims, and that the application is now in condition for allowance. I hope that you agree.